257-335 MR

[redacted]

5264719

SERIAL NUMBER (Series of 1987)	PATENT DATE	PATENT NUMBER
07/705509	NOV 23 1993	5264719

SERIAL NUMBER	FILING DATE	CLASS	SUBCLASS	GROUP ART UNIT	
07/705,509	05/24/91 RULE 60	357	22	258	Potter

APPLICANTS

JAMES D. BEASOM, MELBOURNE VILLA, FL.

CONTINUING DATA********
VERIFIED
THIS APPLN IS A CON OF 07/242,405 09/08/88 Now Abandoned
CIP of 06/831,384 01/07/86 Now US PN 4823173

FOREIGN/PCT APPLICATIONS********None
VERIFIED

FOREIGN FILING LICENSE GRANTED 06/11/91

Foreign priority claimed 35 USC 119 conditions met	AS FILED	STATE OR COUNTRY	SHEETS DRWGS.	TOTAL CLAIMS	INDEP. CLAIMS	FILING FEE RECEIVED	ATTORNEY'S DOCKET NO.
☐ yes ☑ no / ☐ yes ☑ no		FL	10	1	1	$1,420.00	118/2350800

Verified and Acknowledged Examiner's initials

ADDRESS

~~SVENSON, WANDS, EDWARDS, LENAHAN &~~ Law Offices of Charles E. Wands
~~MC KEOWN~~
5240 BABCOCK STREET, NE, STE. 206
PALM BAY, FL 32905

TITLE

HIGH VOLTAGE LATERAL SEMICONDUCTOR DEVICE

U.S. DEPT. of COMM.-Pat. & TM Office—PTO-436L (rev. 10-78)

9m10/19/92

ISSUE FEE IN FILE

PARTS OF APPLICATION FILED SEPARATELY

NOTICE OF ALLOWANCE MAILED	PREPARED FOR ISSUE	CLAIMS ALLOWED
10/28/92	Roy Potter, Assistant Examiner; DM 10/20/92, Docket Clerk	Total Claims 42; Print Claim 1
ISSUE FEE	ROLF HILLE, SUPERVISORY PATENT EXAMINER, ART UNIT 258; Primary Examiner	**DRAWING**
Amount Due $1170.00; Date Paid 1-25-93		Sheets Drwg. 10; Figs. Drwg. 15; Print Fig. 13
Label Area	**ISSUE CLASSIFICATION** Class 257; Subclass 335	ISSUE BATCH NUMBER 431

WARNING: The information disclosed herein may be restricted. Unauthorized disclosure may be prohibited by the United States Code Title 35, Sections 122, 181 and 368. Possession outside the U.S. Patent & Trademark Office is restricted to authorized employees and contractors only.

Form PTO-436 Rev. 9/90

Case No. 04-1371-JJF
DEFT Exhibit No. DX 542
Date Entered _____
Signature _____

FCS1688900

PATENT APPLICATION SERIAL NO. 07/705509

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE
FEE RECORD SHEET

PTO-1556
(5/87)

705509

I hereby certify that this document is being deposited with the United States Postal Service "EXPRESS MAIL POST OFFICE TO ADDRESSEE" service under 37 C.F.R. Section 1.10 and is addressed to the Hon. Commissioner of Patents and Trademarks, Washington, D.C. 20231.
Date: 5/24/91 By: C. N. Ewell
Express Mail No.: FR123690597US

Attorney Docket SE-395CIPX

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

INVENTOR: JAMES D. BEASOM

501

INVENTION: A HIGH VOLTAGE LATERAL SEMICONDUCTOR DEVICE

SPECIFICATION

To All Whom It May Concern:

Be it known that I, James D. Beasom, a citizen of the United States of America, residing at 506 S. Wildwood Lane, Melbourne Village, Florida 32904, have invented certain new and useful improvements in

A HIGH VOLTAGE LATERAL SEMICONDUCTOR DEVICE

of which the following is a specification.

705509

~~Attorney Docket SE-395CIPX~~

Last > B1

FIELD OF THE INVENTION

~~This is a continuation-in-part to the Application Serial No. 831,384, Filed January 7, 1986.~~

The present invention relates to lateral semiconductor devices and an improved method of making lateral semiconductor devices. More specifically, the invention relates to high voltage lateral devices with reduced ON resistance and a method of making such devices.

Previous high voltage lateral devices include both MOS devices and bipolar transistors. For example, Figure 1 illustrates a known structure which can be used as a high voltage lateral MOS device. This device is known as a lateral drift region MOS device and is dependent upon the ~~drain-body~~ drain-to-body junction 15 as the basic high voltage junction of the device. The drift region 17 is a P region along the top surface of the N^- substrate 11 and is located so as to lie adjacent the P^- drain region 12. The drift region 17 is used to connect the high voltage drain 12 to the gate 16 and source 14. The two contacts, drain contact 12_a and body contact 11_c are shown for completeness. In the operation of this circuit, the gate 16 and source 14 never assume large voltages relative to the body 11. The drift region 17

serves as a JFET channel with the portion 11_a of body region 11 underlying the channel acting as a JFET gate. The JFET channel 17 is designed to totally deplete when the drain 12 is reverse biased to a voltage less than the voltage necessary to reach critical field in the ~~channel-to-body~~ channel-to-body depletion layer. This design preserves the effective high breakdown voltage of drain body junction 15. Also the source 14 and gate 16 (over the gate oxide 13) are safely shielded from the high drain body voltage by the pinched off JFET channel 17.

The resistance of the lateral drift region JFET channel 17 is in series with the resistance of the MOS channel 11_b, consequently the total channel resistance of the device is the sum of these two individual resistances. The JFET channel, which must be quite long to sustain high drain body voltages, is often the larger of the two resistance terms. Thus it is desirable to find ways to reduce the resistance of the drift region so that devices of a given size can be made with smaller channel resistance.

Figure 2 illustrates a known structure which can be used as a high voltage lateral DMOS (LDMOS) device. In this device, an N^+ drain ~~12~~ contact 12A is formed in the N^- substrate 211 and an N^+ source 14 and P^+ body contact 11_c are formed in a P^- body region 240. The drift region 217 is an N^- region along the top surface of the N^- substrate 211 which connects the drain 12 to the gate

16 and source 14. In this high voltage device, the N^- drift region 217 must be lightly doped to obtain high body 240 to drain breakdown.

The ON resistance of the LDMOS is approximately the sum of the channel resistance and the bulk resistance in the N^- drift region 217. The lateral distance from the N^+ drain 12 to the adjacent edge of the MOS channel 11_b underlying the gate on the P^- body 240 must be large to allow space for the reverse bias depletion layer which spreads from the body-drain junction into the lightly doped drain. This distance, along with the high N^- resistivity contribute to the high drift region resistance, which is often much greater than the channel resistance. Thus, it is desirable to reduce the drift region resistance of the LDMOS device.

Figure 3 shows a known structure which can be used as a lateral bipolar transistor. Another illustration of such a device is contained in Figure 7 of U.S. Patent No. 4,283,236 issued August 11, 1981. Referring to Figure 3, an N^- substrate 11, has an N type emitter shield 121 formed therein and P^+ emitter 122 and collector 124 formed as shown. Additionally, a P^- drift region 123 is provided along the surface of the substrate between the collector 124 and the emitter shield 121. In the operation of this device, the total collector resistance is equal to the sum of the resistance across the drift region 125 plus the resistance of the P+ collector between the

drift region and the collector contact. In order to provide devices of equal size having a lower collector resistance, it is desirable to find ways to reduce the resistance of the drift region.

In the operation of this device, the drift region extends the collector to the edge of the emitter shield, 121, so that the base width is just that small distance between the adjacent edges of the emitter, 121, and the drift region, therefore, providing improved frequency response.

At high base-collector voltages, the drift region, 123, depletes by JFET action with the N-base, 11, and N shield, 121, which is part of the base, acting as gate before critical field is reached just as for the MOS of Figure 1. This preserves the high breakdown of the structure.

~~Attorney Docket SE-J95CIPX~~

SUMMARY OF THE INVENTION

The present invention provides a structure having a reduced channel resistance and a process capable of efficiently obtaining the structure of the invention. The reduction in channel resistance is accomplished by providing a top gate which is located between the lateral drift region of the prior art and the surface of the channel region and which may be in contact with the high voltage device region. This top gate allows the total channel doping to be increased because the top gate to channel depletion layer holds some additional channel charge when reverse biased in addition to that held by the bottom gate to channel depletion layer of the prior art structure. The ionized channel impurity atoms associated with this additional charnel charge causes the reduction in channel resistance.

With respect to providing an improved LDMOS structure having a lower drift region resistance, a second drift region which is separated from the original drift region by a region of opposing conductivity is formed. The second drift region provides a conductive path which is in parallel with the original drift region thereby achieving the desired reduction in resistance. Because of the formation of the second drift region, the first enclosed drift region can now have a much higher doping than the second drift region which it replaces, while achieving the same breakdown voltage.

~~Attorney Docket SC-3956IPX~~

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a cross section of a known MOS device having typical ON resistance.

Figure 2 is a cross section of a known LDMOS device having typical ON resistance.

Figure 3 is a cross section of a known bipolar transistor having typical collector resistance.

Figure 4 is a cross section of an MOS device including the improved drift region and top gate of the invention.

Figure 5 illustrates optimized process steps for obtaining the desired shape of the top gate and drift region of the invention.

Figures 6a and 6b are, respectively, a top view and a cutaway perspective view of the body contact extending through the top gate and drift region of the invention.

Figure 7 is a cross section of a bipolar device made in accordance with one aspect of the invention.

Figure 8 is a cross section of a bipolar device made in accordance with another aspect of the invention.

Figure 9 is a cross section of a bipolar device made in accordance with a preferred aspect of the invention.

Figure 10 is a cross section of an MOS device, including the lateral drift region and top gate of the invention, in a preferred embodiment.

Figure 11 is a cross section of a LDMOS device made in accordance with a preferred embodiment of the invetion.

Figure 12 is a top view of the LDMOS device of Figure 11.

Figure 13 is a cross section of a LDMOS device made in accordance with another preferred embodiment of the invention.

Figure 14 is a cross section of a LDMOS device made in accordance with still another preferred embodiment of the invention.

~~Attorney Docket SE 395CIPX~~

DETAILED DESCRIPTION OF THE INVENTION

The present invention is described herein with reference to the drawings for both MOS and bipolar applications. Figure 4 shows an MOS device where P^+ drain contact 12_a is formed in P^- type drain 12, P^+ source 14 is formed in the N^- body 11 and N^+ body contact 11_c is provided in the N^- body 11. The MOS channel region 11_b is in the N^- body 11 below the MOS gate 16. The N type top gate 21 is provided along the surface 11_s of the body 11 above the P type drift region 17 which acts as a JFET channel. The lateral edge or peripheral edge of both the top gate 21 and drift region 17 extend to the ~~drain-body~~ drain-to-body junction 15 and preferably terminate at the junction 15. It is noted that situations may exist where the doping level in the top gate may be sufficiently high so as to render it desirable to provide a shorter top gate having a lateral extension which stops short of contacting the junction 15. In this case care should be taken to insure that any nondepleted portion of the top gate does not result in a breakdown of the top ~~gate to drift~~ gate-to-drift region junction 17A. Proper doping of the top gate 21 will generally be a sufficient preventative step. Dashed line 21_p designates the peripheral edge of top gate 21 in an embodiment where the top gate does not extend all the way to the junction 15.

~~Attorney Docket SE-395CIPX~~

The structure of Figure 4 provides reduced ON resistance in the JFET channel relative to the prior art lateral drift MOS device as shown in Figure 1. The reduction in ON resistance is accomplished by providing a structure which can accommodate increased drift region doping without suffering from reduced ~~body to drain~~ body-to-drain breakdown. This is possible because of the provision of the top gate 21. The top ~~gate to channel~~ gate-to-channel depletion layer which holds some channel charge when reverse biased, is in ~~addition~~ addition to the channel charge held by the bottom gate to channel depletion layer of the prior art. This additional channel charge, in the form of ionized channel impurity atoms, causes the reduction in channel resistance. It is possible to provide more than twice the doping level previously acceptable due to the additional ability to hold channel change. Thus, for a drift region having a doping of 1×10^{12} boron atoms per square centimeter in a bottom gate arrangement, the present invention will permit 2×10^{12} boron atoms per square centimeter. Thus, the ON resistance will be only half the ON resistance of the prior arrangement.

In order to optimize performance of the structure of the invention, the top gate 21 must be designed differently than an ordinary JFET gate. Top gate 21 should become totally depleted at a ~~body to drain~~ body-to-drain voltage of less than the breakdown voltage of the top ~~gate to drain~~ gate-to-drain junction 15_a. Since top gate 21 is connected to body 11, the voltage at the top ~~gate to drain~~ gate-to-drain

junction 15_a will equal the voltage of the ~~body to drain~~ body-to-drain junction 15 voltage and the top ~~gate to drain~~ gate-to-drain breakdown voltage should be greater than the voltage at which top gate 21 becomes totally depleted. Additionally, the top gate 21 must totally deplete before the body 11 to channel 17 depletion layer reaches the top gate 21 to channel 17 depletion layer to thereby assure that a large top gate 21 to drain 12 voltage is not developed by punch-through action from the body 11. An ordinary JFET gate never totally depletes regardless of operating conditions.

In addition to the above described characteristics of the device of the invention, it is also necessary to insure that the channel of the JFET drift region 17 contacts the inversion layer MOS surface channel. This can be accomplished as shown in Figure 5 where an implant mask 50 having a tapered edge 51 is provided over the body 11. An implant aperture 52 is provided in mask 50 at the location where the P drift region 17 and top gate 21 are to be formed. The aperture 52 is shown as exposing the protective oxide 53. Ion implantation is not substantially ~~effected~~ affected by the oxide 53 due to the oxide thickness of only about 0.1-0.2 micrometers, yet the oxide provides surface passivation for the underlying body 11.

~~Attorney Docket SE-395CIPX~~

The drift region 17 is ion implanted and, because of the graduated thickness of the implant mask 50 (along the edge 51), the depth of the implanted drift region 17 is graduated or tapered. In the illustration, a fairly good rounding of the drift region 17 occurs at the peripheral edges or extremeties 17_a, 17_b of the region 17. The curved extremity 17_a is of interest because at this location the channel of the JFET drift region 17 contacts the surface 11_s of body 11 beyond the end 21_a of top gate 21 and is desirably beneath the gate 16 of the MOS device. The top gate 21 may be ~~ion implanted~~ ion-implanted using the implant mask 50 but at an energy level which results in a shallower implantation. This tapered profile, particularly if curved, provides improved performance.

In a variation of this method, a diffusion process can be used to bring the JFET channel into contact with the surface of body 11, and hence insure that the JFET channel 17 will contact the inversion layer MOS surface channel (lateral drift region 17 and top gate 21 are diffused after initial introduction by ion implant). The doping levels and diffusion times are chosen such that the extremity 17_a of JFET channel 17 diffuses beyond the end 21_a of the top gate 21 and so that the end 17_a reaches the surface 11_s of body 11. In practice, this approach can be facilitated by choosing a top gate dopant which has a lower diffusion coefficient than that of the drift region dopant.

~~Attorney Docket SC-395CIPX~~

The formation of the drift region 17 and top gate 21 may be conveniently carried out by forming a mask over the gate oxide which is present in a lateral MOS application. The MOS gate may be utilized as one delineating edge of the implant for the drift region and top gate and a thick oxide portion surrounding a thinner oxide portion may form the remainder of the implant mask. The thinner oxide portion shall be located such that it extends from beneath the MOS gate to the drain and preferably overlaps the drain. The implant mask 50 illustrated in Figure 5 is shown as having thin oxide portion 53 being surrounded by the implant mask 50. If the MOS gate 16 shown in dashed lines were used as a portion of the mask 50, the edge of the drift region and top gate would be self-aligned with the MOS gate as shown in dashed lines. Then, when diffused, the drift region will extend laterally to a point beneath the MOS gate, while the top gate 21 may be formed such that there is little or no lateral overlap with the MOS gate. The extent of lateral diffusion of the top gate is dependent upon the dopant material and processing temperatures following top gate implant. It is noted that there is a separation between the drift region and the source. This separation zone is the location where the MOS channel is located.

The top gate 21 will perform as previously described if it is tied to the body 11. Thus, the top gate 21 and the body which operates as the bottom gate of the JFET channel will be at equal potential. According to the

~~Attorney Docket SE-395CIPX~~

invention, this may be accomplished in a particularly effective manner if the drift region 17 is widened to overlap with the body contact region 11_c. This is shown in Figure 6a which shows the overlapping of the top gate 21 and the body contact 11_c at the overlap regions 21_c, 21_d. In order for this arrangement to be effective, it is necessary that the body contact 11_c have a higher dopant concentration than the JFET channel (or drift region) 17, as shown in Figure 6b to insure that the body contact 11_c forms a continuous region horizontally and/or vertically through the JFET channel and to the body region 11 from the top gate, 21.

Figure 6b shows a cross section of the structure of Figure 6a taken along dashed line A-A. The body 11 is provided with body contact 11_c which is located such that the top gate 21 and drift region 17 can be conveniently extended to overlap the body contact 11_c. The depth of body contact 11_c may be made greater than the depth of region 17 such that a portion of the body contact 11_c extends below region 17 and provides contact with the body 11. This arrangement provides a contact portion 21_c where the top gate 21 is in contact with body contact 11_c. Thus, ~~so~~ as long as the body contact doping concentration in region 21_b is sufficiently high to overcome the opposite doping in region 17, then a good connection of uniform conductivity type will be provided between the top gate 21 and the body 11, via contact region 11c. It is also noted that the body contact 11_c extends laterally beyond the end

of both of the top gate 21 and the drift region 17. The lateral extension of the contact 11_c will also provide a structure which results in a good connection of uniform conductivity type from the top gate 21 to the body 11, again, provided that the doping of body contact 11_c converts region 21_b.

Another area where the present invention finds application is in lateral bipolar transistors which employ a lateral drift region. The known structure of Figure 3 may be improved by providing an N type top gate 126 as shown in Figure 7. In this arrangement the N type top gate 126 extends from the collector 124 to the emitter shield 121 along the surface of body 11. The operation of this device is enhanced by the same phenomenon as the lateral drift region of the previously described MOS device. As the base 11 becomes positive relative to the collector 124, the top gate-to-drift region depletion layer facilitates pinch-off of the drift region 123. However, as the base 11 becomes more negative, the top gate 126 contributes additional surface exposure to the drift region 123 and further enhances carrier transportation.

Figure 8 shows an improvement over the arrangement shown in Figure 7. In Figure 8 the drift region 123 does not extend all the way over to the emitter shield 121. The curved end 123_a of the drift region 123 contacts

the top surface of body 11. It is noted that in this arrangement, the emitter shield 121 may be omitted.

An additional improvement shown in Figure 8 is the use of a deep diffusion to form the collector 124 resulting in a significantly increased breakdown voltage. The deep diffusion step may be the same step used for forming the emitter, in which case the collector 124 shown in Figure 7 would be deeper, or a separate collector implant and diffusion step may be employed and the collector contact 127 may then be formed simultaneously with the formation of the emitter 122. This improvement in junction breakdown voltage is equally obtainable, for example, at the body to drain junction in the MOS devices described previously.

A further extension of the invention which may be used to increase base-to-collector breakdown voltage for a PNP device is shown in Figure 9. In addition to the provision of the N type top gate 126_a over the P^- drift region 123_a, the top gate 126A and drift region 123A are enlarged to surround the collector 124 and a curved edge 123_e is provided at the periphery of the enlarged portion 123_b of the drift region 123A. This enlarged portion is designated by reference numerals 123_b for the drift region and 126_b for the top gate. The collector 124 to base 11 breakdown voltage is increased relative to alternative arrangements because of mitigation of the breakdown

~~Attorney Docket SE-396CIPX~~

reduction due to the junction curvature. The top gate 126_a extends to the emitter shield 121 as does the drift region 123_a. The P^+ emitter 122 is formed in the N^+ type emitter shield 121.

Figure 10 illustrates an extension of the invention with respect to a P channel MOS device similar to the improvement described with respect to the bipolar device shown in Figure 9. For the MOS device, the drain 12 is surrounded by the P^- drift region 17 and N type top gate 21. Around the entire periphery of the drift region 17 there is a curved portion 17_e which rounds up to the surface of the N^- substrate 11 to insure that the JFET channel in the drift region 17 contacts the MOS channel 11_b under the MOS gate 16. The drift region 17 extends outward from the entire perimeter of the drain 12. This arrangement mitigates the breakdown reduction due to junction curvature. The P^+ source 14 and N^+ body contact 11_c are shown as is the dielectric 13 which serves as the gate oxide 13_g beneath the MOS gate 16.

In both the arrangements shown in Figure 9 and Figure 10, the planar diode breakdown improvement created by the drift region acting as a surface layer of the same conductivity type as the collector in Figure 9 and drain in Figure 10 and extending out from the perimeter of the collector and drain can be implemented by a single series of process steps. According to the

~~Attorney Docket SC-395CIPX~~

invention, a common set of process steps produces both a suitable breakdown improvement layer and an improved drift region. The breakdown improvement layer is a two layer component.

A further extension of the invention is illustrated in Figure 11 which shows an LDMOS device where N^+ drain contact 12_a is formed in an N^- type substrate and an N^+ source 14 and P^+ body contact 11c are formed in a P^- type body region 240. The DMOS channel region 11_b is in the P^- body 240 below the DMOS gate 16. The N type first drift region 217 is provided along the surface 11_s of the substrate 11 above a P^- type separation region 250. A second drift region 217_a exists in the substrate 11 underneath the P^- type separation region. The lateral edge of both the first drift region 217 and the separation region 250 extend from the gate 16 to the N^+ drain contact 12_a.

The structure in Figure 11 provides reduced ON resistance by way of (surface) 217A drift region ~~217a~~ relative to the (deeper) prior art lateral first drift region device ~~as shown~~ refer to above in Figure 2. To illustrate this, consider an example in which the N^- region 11 has a doping of 1×10^{14} ions cm^{-3}. The top gate layer 217 has an integrated doping of about 1×10^{12} ions cm^{-2} and is preferably not more than two microns thick while maintaining full breakdown. The thickness of the N and P layers 217, 250 together is preferably less than

~~Attorney Docket SE-395CIPX~~

ten microns and can be less than one micron. The same integrated doping in the N- ~~region~~ body 11 requires a thickness of 100 microns. Thus, the N and P layers 217, 250 respectively consume only a small fraction of the N- thickness required to provide doping equal to that portion of the N layer of the prior art device.

The lateral spacing between the drain contact 12_a and the channel 11_b in the device described above would be approximately 30 microns. In such a device, even if a full 100 micron thick N- ~~region~~ body 11 were provided, it would have a higher resistance than the N- ~~region~~ first drift region 217 provided according to the invention. This is because the average path length of current flowing from the drain contact 12A down through the thick N- ~~region~~ body 11 and back up to the surface edge of the channel at the ~~drain-body~~ drain-to-body junction would be greater than the direct path through the N- region first drift 11.

Maximum breakdown is achieved in the invention by providing doping densities of the N and P layers 217, 250 such that they become totally depleted before breakdown is reached at any point along the junctions which they form with adjoining regions and before breakdown is reached at the junction between them. To insure that this occurs, the N region 217 should have an integrated doping not exceeding approximately 1×10^{12} ions cm^{-2} and the P region 250 should have a higher integrated doping not exceeding about 1.5 to 2×10^{12} ions cm^{-2}.

~~Attorney Docket SE-395CIPX~~

To insure proper depletion of the P and N regions 250, 217, they must have the proper voltages applied. The N layer bias is achieved by connecting the N ~~layer~~ 217 to the higher concentration N^+ drain contact 12_a by overlapping the N ~~layer~~ 217 and drain contact 12_a. The P ~~layer~~ 250 bias is achieved by overlapping the P ~~layer~~ with the P^- body 240 at least at one end of the channel, thereby applying the body voltage to the P layer 250. This is illustrated in Figure 12.

With this structure and choice of doping levels, the desired results are achieved. When a reverse bias voltage is applied to the ~~drain-body~~ junction, the same reverse bias appears on both the ~~P and N-~~ junction 260 and the ~~P to N-~~ junction 270. Depletion layers spread up into the ~~N-~~ and down into the N^- ~~regions~~ from the P layer. In a preferred embodiment, the P and N ~~layer~~ dopings are chosen such that the N layer 217 becomes totally depleted at a lower voltage than that at which the P layer 250 becomes totally depleted. This insures that no residual undepleted portion of the N layer 217 is present which could reduce breakdown voltage.

As a result of the invention, the improved DMOS device provides a reduced resistance current path in the drain which does not depend on the N^- doping. This allows the N^- doping to be reduced to achieve a desired breakdown

voltage with good manufacturing margin, while maintaining desirable low drift region resistance. In a multi-device process which includes LDMOS devices, the N- region can be adjusted to achieve the desired characteristics of one or more of the other device types, while the N ~~layer~~ first drift region 217 sets the drift region 217 resistance of the LDMOS.

Another embodiment of the DMOS invention is illustrated in Figure 13, where the N and P ~~layers~~ regions 217, ~~250~~ 231 are self-aligned to the gate 16 by using the gate 16 as a mask. An advantage of this structure is that N and P regions can be defined by the uncovered thin oxide area which extends from gate edge to overlap the drain contact. This embodiment requires no explicit mask step to delineate the location where the N and P regions are formed.

Still another embodiment, as illustrated in Figure 14, provides no gap between the P- body 240 and the P region ~~250~~ 231 adjacent to the channel edge. The absence of the gap prevents current from flowing in the N- ~~region~~ body 11, so the entire drift region current path is in the N ~~region~~ first drift region 217. Elimination of the gap also allows the device structure to be made smaller. As with the other structure, the N and P regions may be self-aligned to the gate edge, as illustrated in Figure 14, or not self-aligned. They may also be covered by thick or thin oxide as a design option.

A preferred feature of the present invention provides that the body or substrate regions 11 shown in the Figures 3, 4, 6,7, 8, 9, 11, 13 and 14 are designed to be dielectrically or self-isolated regions. In contrast with the typical RESERF type of devices in which the bottom isolation junction plays a central role in the action of the device, the present invention contemplates that the isolation junction does not contribute to the depletion of the drift or top gate regions which are taught to be totally depleted. Prior art RESERF devices such as that described in U. S. Patent No. 4,300,150 to Colak always require the substrate to be part of such depletion whereby the substrate must assume the most negative voltage in the device because of its role as one side of the isolation junction. As a result of this bias on the substrate or body region, the prior art RESERF type devices are susceptible to punch through from the device region through the epitaxial layer to the substrate. As a result of the present invention not having the substrate as part of the depletion mechanism, the invention can more effectively provide high voltage protection while not increasing the resistance of the channel path. Although the figures illustrate a nonisolating structure or self-isolated structure, it is understood that the invention applies equally well to dielectrically or junction isolated substrates.

~~Attorney Docket SE-395C1PX~~

While the present invention has been described with respect to several preferred manners of implementing the invention, it is to be understood that the claims appended hereto are intended to cover the invention in its broadest sense and are not to be limited to the specific implementations disclosed.

~~Attorney Docket SF-395CIPX~~

CI WHAT IS CLAIMED IS:

1. A semiconductor device of the type including a lateral drift region of a first conductivity type formed in a body region, said drift region serving as a JFET channel, the improvement comprising:

a top gate of a semiconductor material having a second conductivity type over said drift region to cause depletion of said drift region from a first surface upon application of a reverse bias voltage to said device,

wherein said top gate laterally abutts a device region to form a junction and has a surface area doping density such that it becomes totally depleted at a reverse bias voltage below the reverse breakdown voltage of the top gate to device region junction, and

wherein said top gate has a surface area doping density such that it becomes totally depleted at a reverse bias voltage less than the reverse bias voltage at which said drift region becomes depleted.

N P N K

~~Attorney Docket SE-395CIPX~~

2. A semiconductor device as claimed in claim 1, wherein said body region is a dielectrically isolated substrate.

3. A semiconductor device as claimed in claim 1, wherein said body region is a junction isolated substrate.

4. A semiconductor device as claimed in claim 2 wherein said drift region has a tapered peripheral edge.

5. A semiconductor device as claimed in claim 4 wherein said top gate has a lateral expanse bounded by said drift region.

6. A semiconductor device as claimed in claim 5 wherein said top gate has a tapered peripheral edge.

7. A semiconductor device comprising:

a substrate of a first conductivity type;

a first device region of a second conductivity type formed in said substrate;

a second device region of said second conductivity type formed in said substrate and separated from said first device region;

a drift region of said second conductivity type formed in said substrate between said first and second device regions, separated from said second device region by a separation zone and in contact with said first device region, said drift region having a first side adjacent said body;

a top gate of said first conductivity type adjacent a substantial portion of a second side of said drift region and electrically connected to said substrate;

said top gate becoming totally depleted at a body to first device region voltage below the voltage at which the semiconductor to drift region depletion layer in said first side of said drift region reaches the top gate to drift region depletion layer in said second side of said drift region.

~~Attorney Docket SC-395CIPX~~

8. A semiconductor device as claimed in claim 7, wherein said substrate is a dielectrically isolated substrate.

9. A semiconductor device as claimed in claim 7, wherein said substrate is a junction isolated.

10. A semiconductor device as claimed in claim 7, wherein said substrate is an isolated island.

11. A semiconductor device as claimed in claim 9 wherein said first device region is a drain of a lateral drift region MOS device;

said semiconductor device further comprising an MOS gate located over said separation zone and overlapping a portion of said drift region.

12. A semiconductor device as claimed in claim 9 wherein said first device region is a collector of a lateral bipolar transistor and wherein said separation zone comprises an emitter shield region of said first conductivity type.

~~Attorney Docket SE-395CIPX~~

13. A semiconductor device as claimed in claim 9 wherein said drift region and top gate are in contact with said first device region about the entire periphery of said first device region.

14. In a lateral MOS structure comprising an isolated semiconductor body of a first conductivity type, source and drain regions of a second conductivity type, and a drift region of said second conductivity type, said drift region forming a JFET channel controlled by said semiconductor body which body operates as a JFET gate such that upon application of a reverse bias to said body to drain junction said drift region becomes depleted, the improvement comprising:

a top gate of said first conductivity type formed over said drift region.

15. A lateral MOS structure as claimed in claim 14 wherein:

said top gate becomes depleted below a body to drain voltage at which the body to channel depletion layer reaches the top gate to channel depletion layer.

~~Attorney Docket SE-395CIPX~~

16. A lateral MOS structure as claimed in claim 15 wherein:

said drift region is formed in said semiconductor body along a top surface of said semiconductor body and said top gate is formed in said drift region along said top surface such that said drift region is between said top gate and said semiconductor body.

17. A lateral MOS structure as claimed in claim 16 wherein:

said drift region extends from said body to said top gate.

18. A lateral MOS structure as claimed in claim 14 wherein:

said top gate is laterally spaced from said drain.

19. A lateral MOS structure as claimed in claim 14 wherein:

a body contact of said first conductivity type is formed in said body and said top gate overlaps said body contact, said body contact having an impurity concentration higher than the impurity concentration of said drift region.

~~Attorney Docket SE-395CIPX~~

20. A lateral MOS structure as claimed in claim 14 wherein:

said drift region and said top gate extend laterally around the entire surface intersection of the drain to body junction to reduce the surface field and thereby increase breakdown voltage of the drain to body junction.

21. A lateral MOS structure as claimed in claim 14 wherein:

said top gate totally depletes below a body to drain voltage at which said drift region totally depletes.

22. A lateral MOS structure as claimed in claim 14 wherein:

said top gate gate is formed by an ion implant, and said top gate has a tapered peripheral edge.

23. A lateral MOS structure as claimed in claim 22 wherein:

said drift region is formed by an ion implant and said drift region has a tapered peripheral edge.

24. A lateral MOS structure as claimed in claim 14 wherein:

said top gate becomes depleted at a body to drain voltage below the breakdown voltage of the junction of said top gate to said drain region.

25. A semiconductor device of the type including a first lateral drift region of a first conductivity type formed in a body region, the improvement comprising:

a separation layer of a second conductivity type formed adjacent to said first lateral drift region;

a second lateral drift region of said first conductivity type separated by the first lateral drift region by said separation layer.

26. A semiconductor device as claimed in claim 25 wherein:

said separation layer and first lateral drift region have surface area doping densities such that the first lateral drift region becomes totally depleted at a lower voltage than that at which the separation layer becomes totally depleted.

~~Attorney Docket SE 395CIPX~~

27. A semiconductor device as claimed in claim 26, wherein said first and second lateral drift regions and said separation region abutt a first device region of said first conductivity type.

28. A semiconductor device as claimed in claim 27, further comprising a second device region of said first conductivity type formed in a body region of said second conductivity type.

29. A semiconductor device as claimed in claim 28, wherein said first drift region and separation region abutt said body region containing said second device region.

30. A semiconductor device as claimed in claim 29, further comprising a gate, wherein a peripheral edge of said gate is aligned with a peripheral edge of said first drift region.

Add A37

765509

~~Attorney Docket SE-395CIPX~~

ABSTRACT

The present invention provides an improved lateral drift region for both bipolar and MOS devices where improved breakdown voltage and low ON resistance are desired. A top gate of the same conductivity type as the device region with which it is associated is provided along the surface of the substrate and overlying the lateral drift region. In an MOS device, the extremity of the lateral drift region curves up to the substrate surface beyond the extremity of the top gate to thereby provide contact between the JFET channel and the MOS channel.

OATH IN PENDING APPLICATION
CONTAINING ADDITIONAL SUBJECT MATTER

ATTORNEY'S DOCKET NO.

I, the below named inventor, hereby swear or affirm that my residence, post office address and citizenship are as stated below next to my name;
that I verily believe that I am the original, first and sole inventor if only one name is listed at 201 below, or a joint inventor if plural inventors are named below at 201-203, of the invention entitled: A HIGH VOLTAGE LATERAL SEMICONDUCTOR DEVICE
which is described and claimed in the attached specification;
that this application in part discloses and claims subject matter disclosed in my earlier filed pending application,

Serial No. 831,384 filed January 7, 1986
that I acknowledge my duty to disclose information of which I am aware which is material to the examination of this application;
that, as to the subject matter of this application which is common to said earlier application, I do not know and do not believe that the same was ever known or used in the United States of America before my or our invention thereof or patented or described in any printed publication in any country before my or our invention thereof, or more than one year prior to said earlier application, or in public use or on sale in the United States of America more than one year prior to said earlier application, or in public use or on sale in the United States of America more than one year prior to said earlier application;
that the common subject matter has not been patented or made the subject of an inventor's certificate issued before the date of said earlier application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months prior to said earlier application; and
as to applications for patents or inventor's certificate on the common subject matter filed in any country foreign to the United States of America prior to said earlier application by me or my legal representatives or assigns,

☒ no such applications have been filed, or

☐ such applications have been filed as follows:

EARLIEST FOREIGN APPLICATION(S), IF ANY, FILED WITHIN 12 MONTHS PRIOR TO SAID EARLIER APPLICATION

COUNTRY	APPLICATION NUMBER	DATE OF FILING (day, month, year)	DATE OF ISSUE (day, month, year)	PRIORITY CLAIMED UNDER 35 U.S.C. 119
				YES ☐ NO ☐
				YES ☐ NO ☐

ALL FOREIGN APPLICATIONS, IF ANY, FILED MORE THAN 12 MONTHS PRIOR TO SAID EARLIER APPLICATION

that as to the subject matter of this application which is not common to said earlier application, I do not know and do not believe that the same was ever known or used in the United States of America before my or our invention thereof or patented or described in any printed publication in any country before my or our invention thereof, or more than one year prior to this application, or in public use or on sale in the United States of America more than one year prior to this application;
that said non-common subject matter has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months prior to this application; and
as to applications for patents or inventor's certificate on the non-common subject matter filed in any country foreign to the United States of America prior to this application by me or my legal representatives or assigns,

☒ no such applications have been filed, or

☐ such applications have been filed as follows:

EARLIEST FOREIGN APPLICATION, IF ANY, FILED WITHIN 12 MONTHS PRIOR TO THIS APPLICATION

COUNTRY	APPLICATION NUMBER	DATE OF FILING (day, month, year)	DATE OF ISSUE (day, month, year)	PRIORITY CLAIMED UNDER 35 USC 119
				☐ YES ☐ NO
				☐ YES ☐ NO

ALL FOREIGN APPLICATIONS, IF ANY, FILED MORE THAN 12 MONTHS PRIOR TO THIS APPLICATION

PTO Form 3.18 Patent and Trademark Office - U.S. DEPARTMENT of COMMERCE

(continued)

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. *(list name and registration no.)*

William A. Troner, Reg. No. 32,316; Les J. Hart, Reg. No. 26,462;
Charles C. Krawczyk, Reg. No. 22,453

SEND CORRESPONDENCE TO:	DIRECT TELEPHONE CALLS TO: *(name and telephone number)*
William A. Troner, Esq. Harris Semiconductor P. O. Box 883, M/S 53-055 Melbourne, Florida 32901	William A. Troner (407) 729-4511

		FAMILY NAME	FIRST GIVEN NAME	SECOND GIVEN NAME
201	FULL NAME OF INVENTOR	Beasom 40100	James	D.
	RESIDENCE & CITIZENSHIP	CITY: Melbourne Village	STATE OR FOREIGN COUNTRY: Florida FL	COUNTRY OF CITIZENSHIP: U. S. A.
	POST OFFICE ADDRESS	POST OFFICE ADDRESS: 506 S. Wildwood Lane	CITY: Melbourne Village	STATE & ZIP CODE/COUNTRY: Florida 32904/USA
202	FULL NAME OF INVENTOR	FAMILY NAME	FIRST GIVEN NAME	SECOND GIVEN NAME
	RESIDENCE & CITIZENSHIP	CITY	STATE OR FOREIGN COUNTRY	COUNTRY OF CITIZENSHIP
	POST OFFICE ADDRESS	POST OFFICE ADDRESS	CITY	STATE & ZIP CODE/COUNTRY
203	FULL NAME OF INVENTOR	FAMILY NAME	FIRST GIVEN NAME	SECOND GIVEN NAME
	RESIDENCE & CITIZENSHIP	CITY	STATE OR FOREIGN COUNTRY	COUNTRY OF CITIZENSHIP
	POST OFFICE ADDRESS	POST OFFICE ADDRESS	CITY	STATE & ZIP CODE/COUNTRY

SIGNATURE OF INVENTOR 201	SIGNATURE OF INVENTOR 202	SIGNATURE OF INVENTOR 203
James D. Beasom		
DATE: September 8, 1988	DATE	DATE

State of Florida)
SS
County of Brevard)

Sworn to and subscribed before me this _____ day of _____, 19 _____.

_____
(signature of notary or officer)

(SEAL)

_____
(official character)

PTO Form 3.18 (page 2) Patent and Trademark Office - U.S. DEPARTMENT of COMMERCE

705509

118/28508X00

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT: James D. Beasom

SERIAL NO.: 242,405 ART UNIT: 258

FILED: September 8, 1988 EXAMINER: F. Abraham

FOR: HIGH VOLTAGE LATERAL SEMICONDUCTOR DEVICE

APPOINTMENT OF ASSOCIATE ATTORNEY

Honorable Commissioner of
Patents and Trademarks
Washington, D.C. 20231

Sir:

The undersigned, a named principal attorney in the above-identified application, hereby appoints as associate attorney, the following attorneys, to prosecute and transact all business in the Patent and Trademark Office connected therewith:

Charles E. Wands - Reg. No. 25,649;
Donald D. Evenson - Reg. No. 26,160;
Gary R. Edwards - Reg. No. 31,824;
James F. McKeown - Reg. No. 25,406;
John A. Hankins - Reg. No. 32,029;
Jeffrey Sanok - Reg. No. 32,169

Please direct all future communications in connection with this application to the following address:

EVENSON, WANDS, EDWARDS, LENAHAN & MCKEOWN
5240 Babcock Street, N.E.
Suite 206
Palm Bay, Florida 32905

Date: July 18, 1990 By: William A. Troner
William A. Troner
Reg. No. 32,316

FIGURE 1

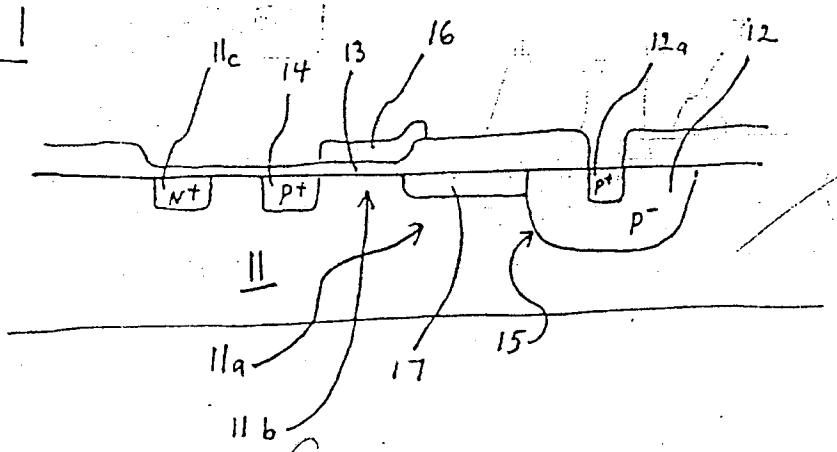


FIGURE 3

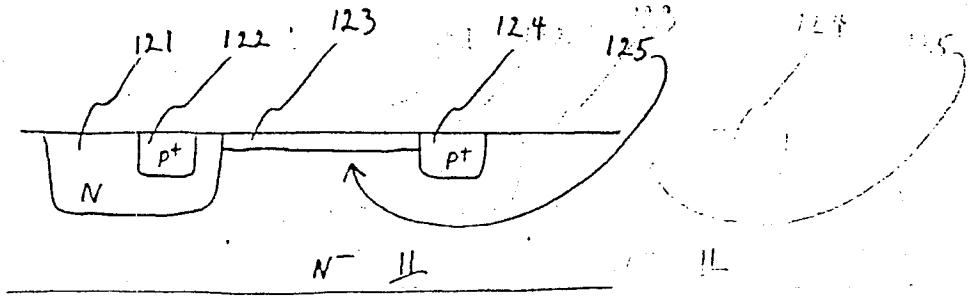


Fig. 15

2/10

Lateral DMOS prior art

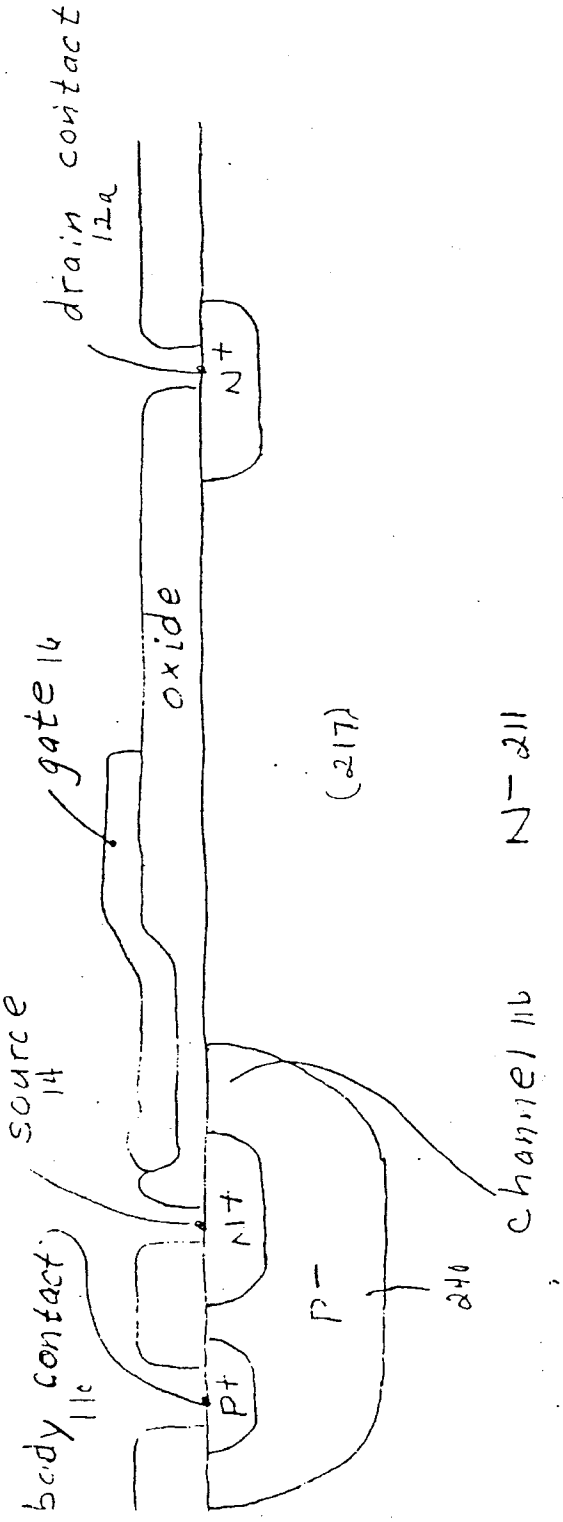


FIGURE 4

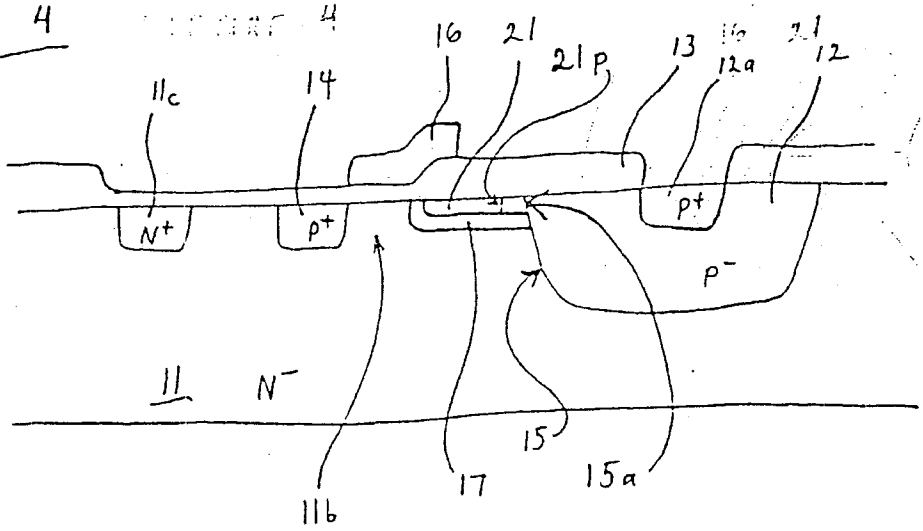


FIGURE 5

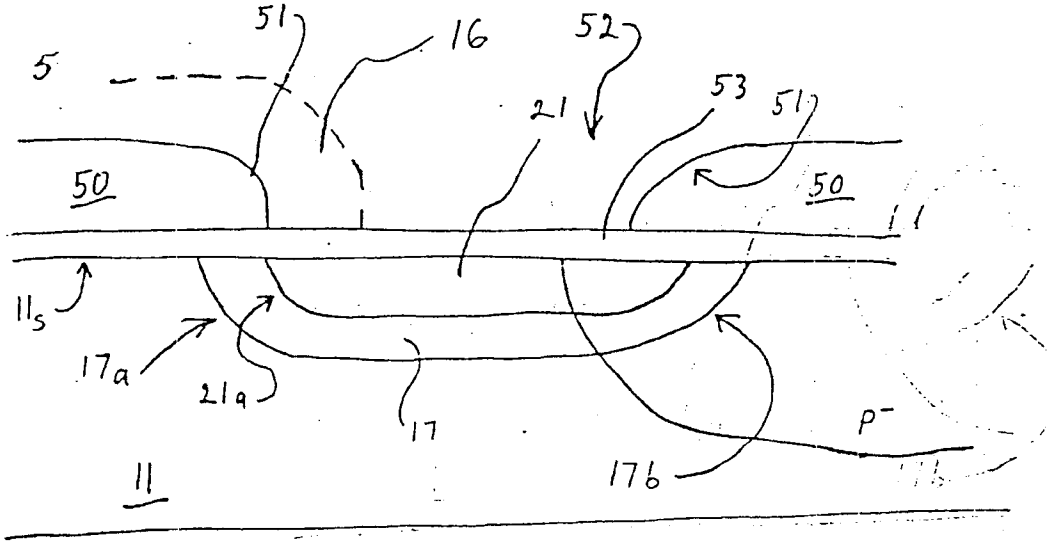


FIGURE 6a

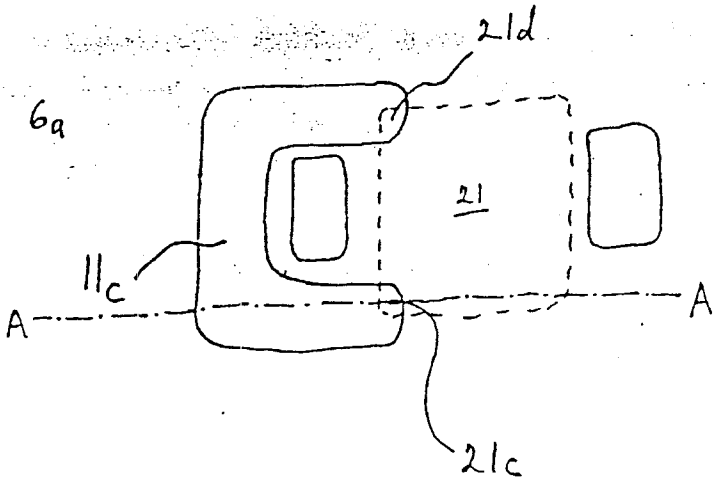
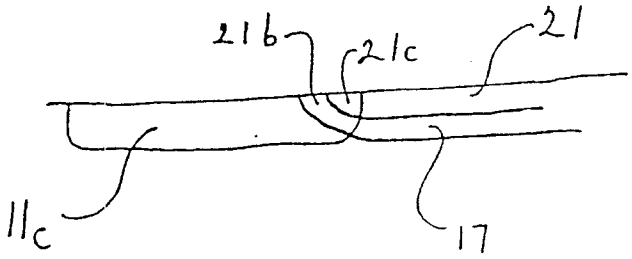


FIGURE 6b



IGURE 7

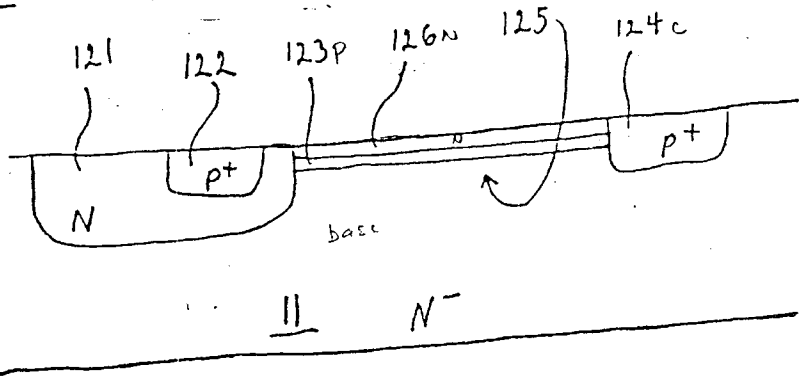
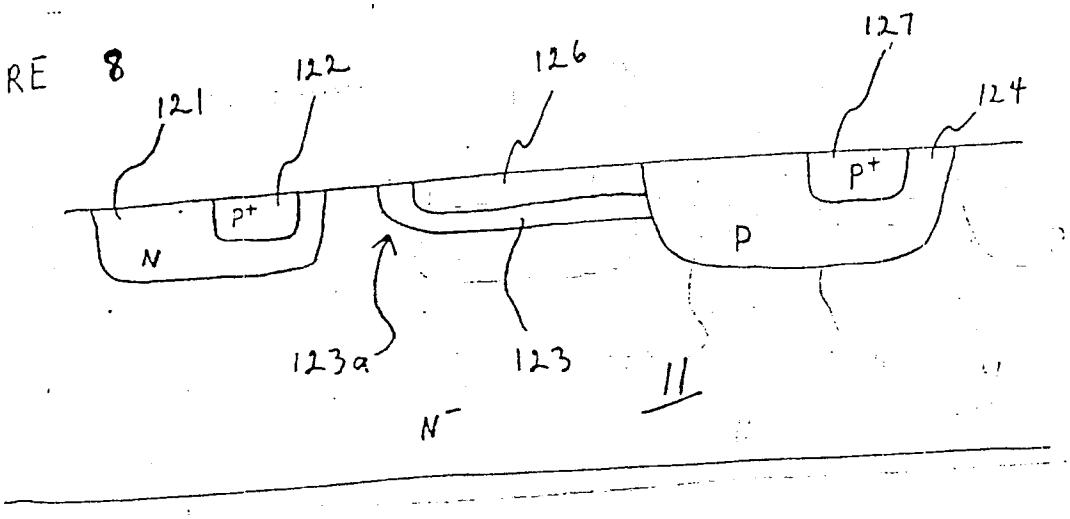


FIGURE 8



6/10

IT/705509

FIGURE 9

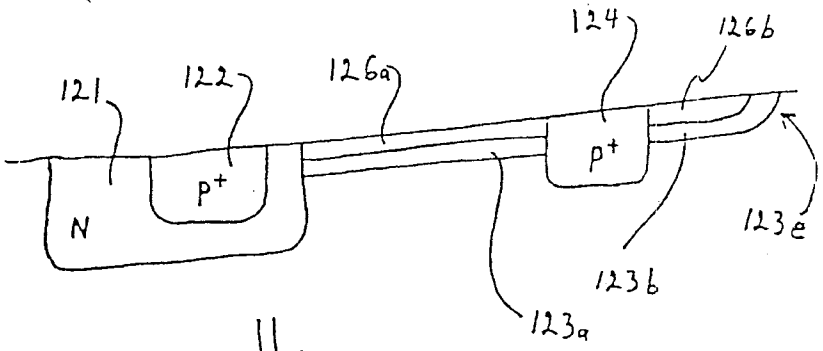
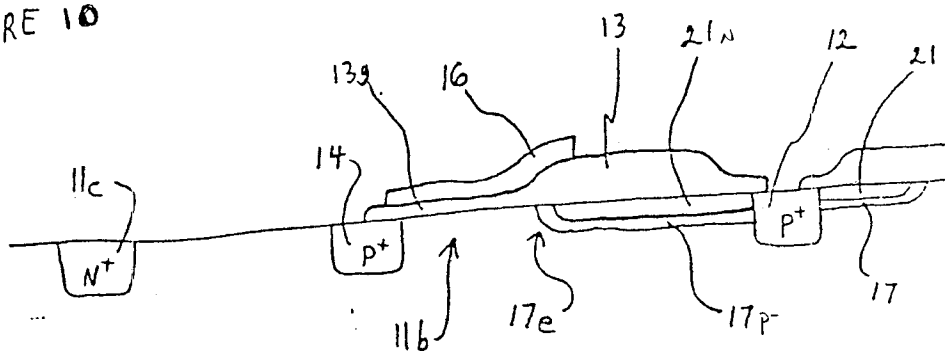
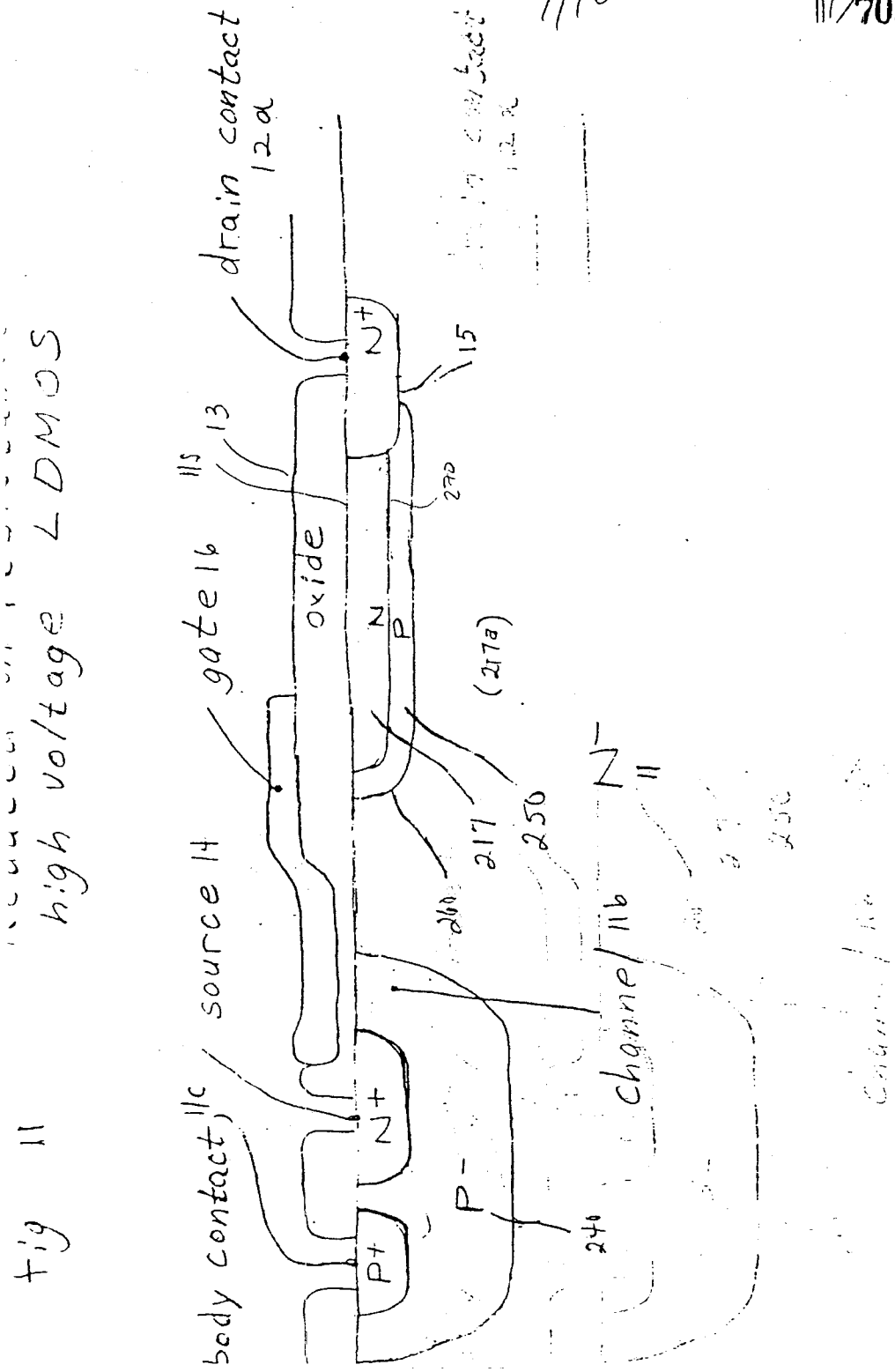


FIGURE 10



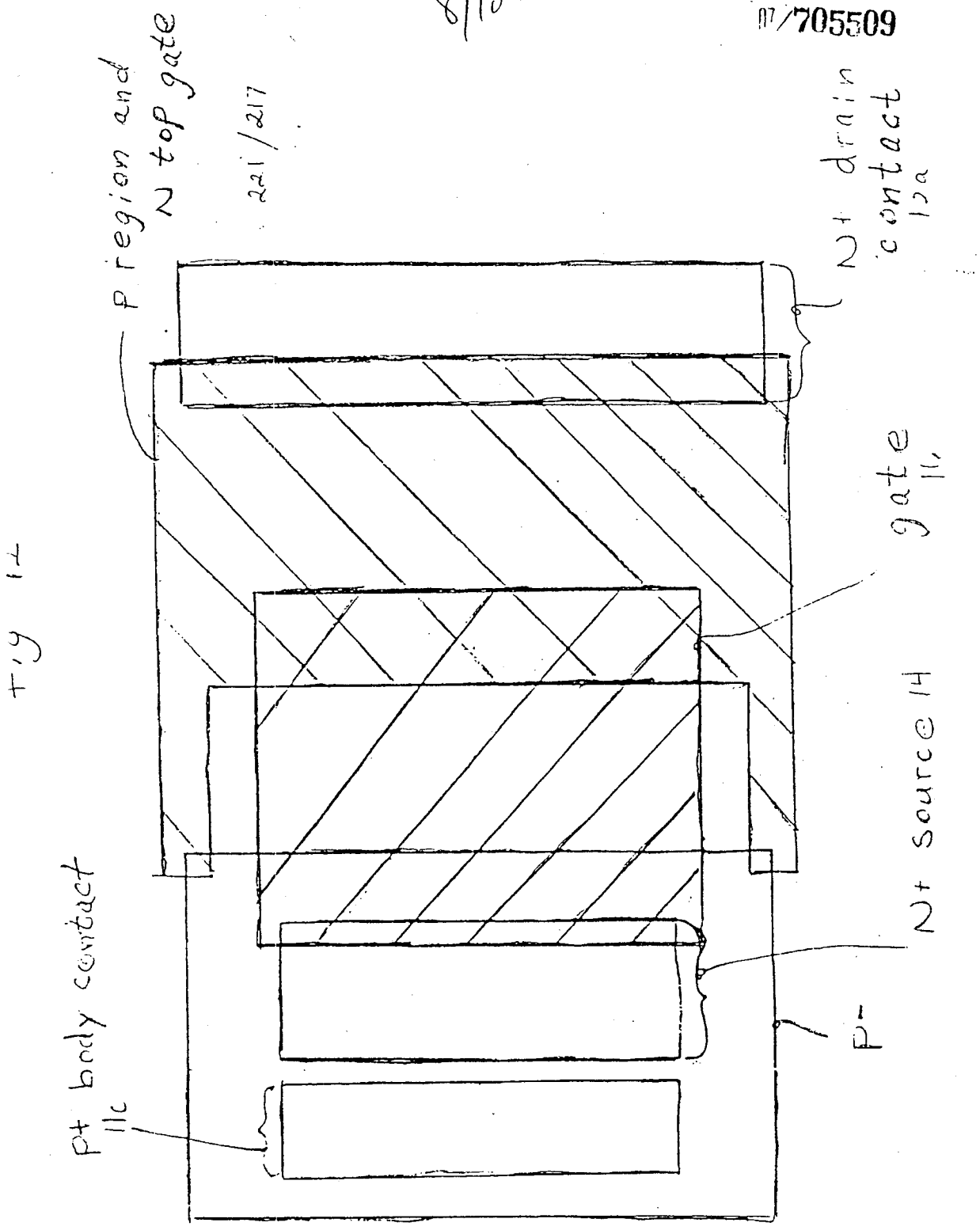
7/10

IT/705509



8/10

11/705509



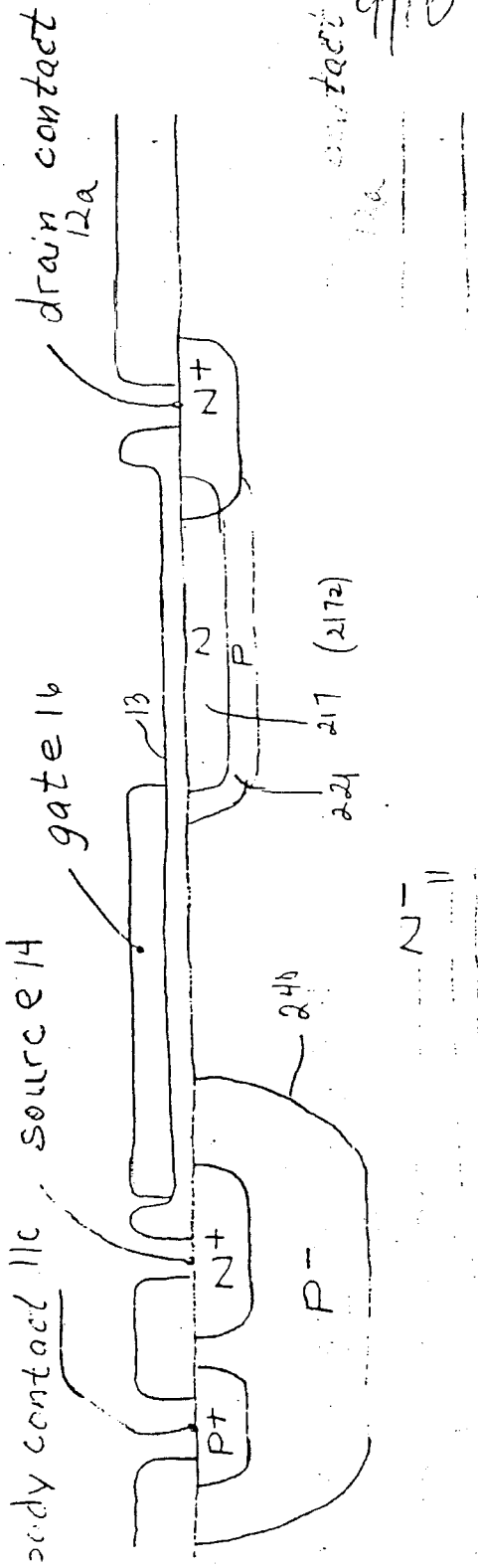
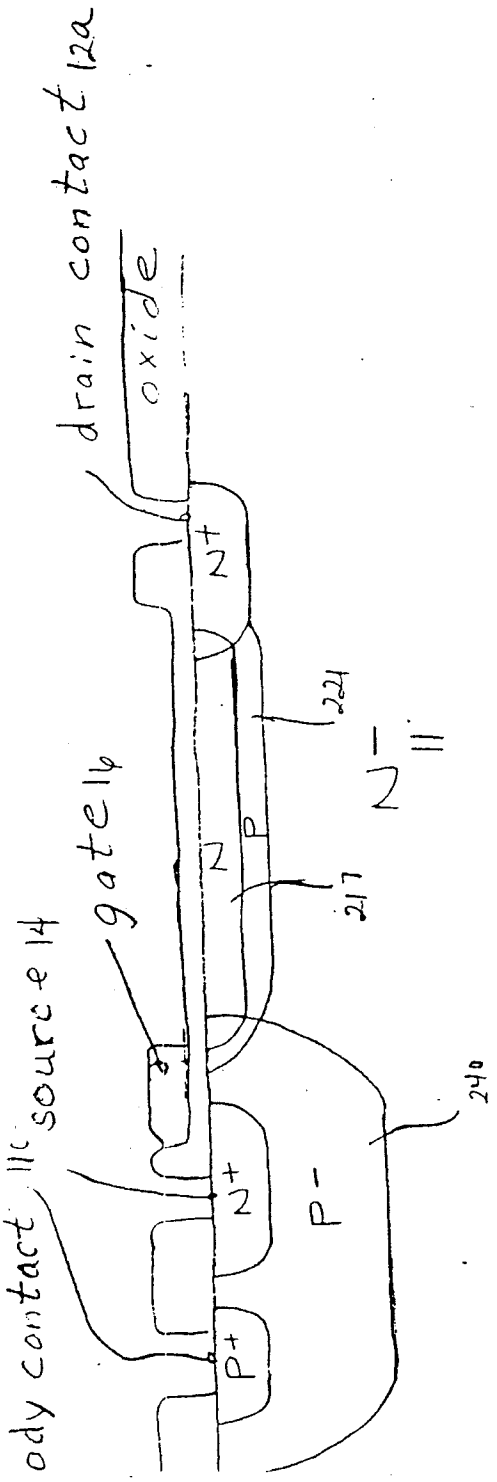

drain contact
12a
gate 16
source 14
body contact 11c
N+
P
N
P+
P-
N-
13
21 (21')
22
24
11

Fig 12

10/10

705509

Fig 14



Print Of Drawings
As Originally Filed

07/705509

FIGURE 1

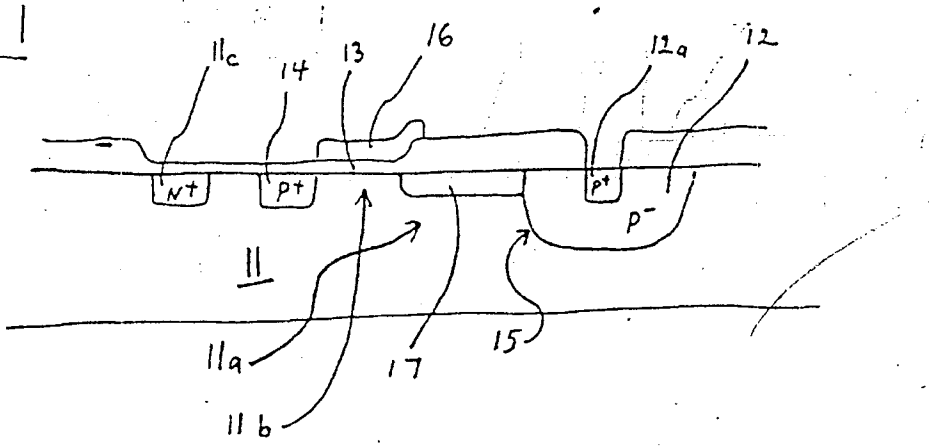
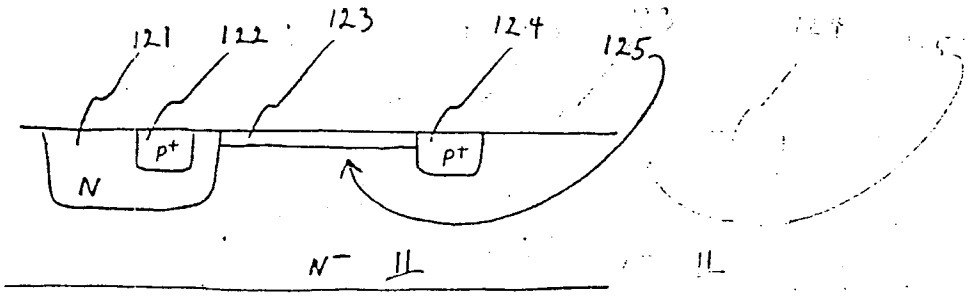


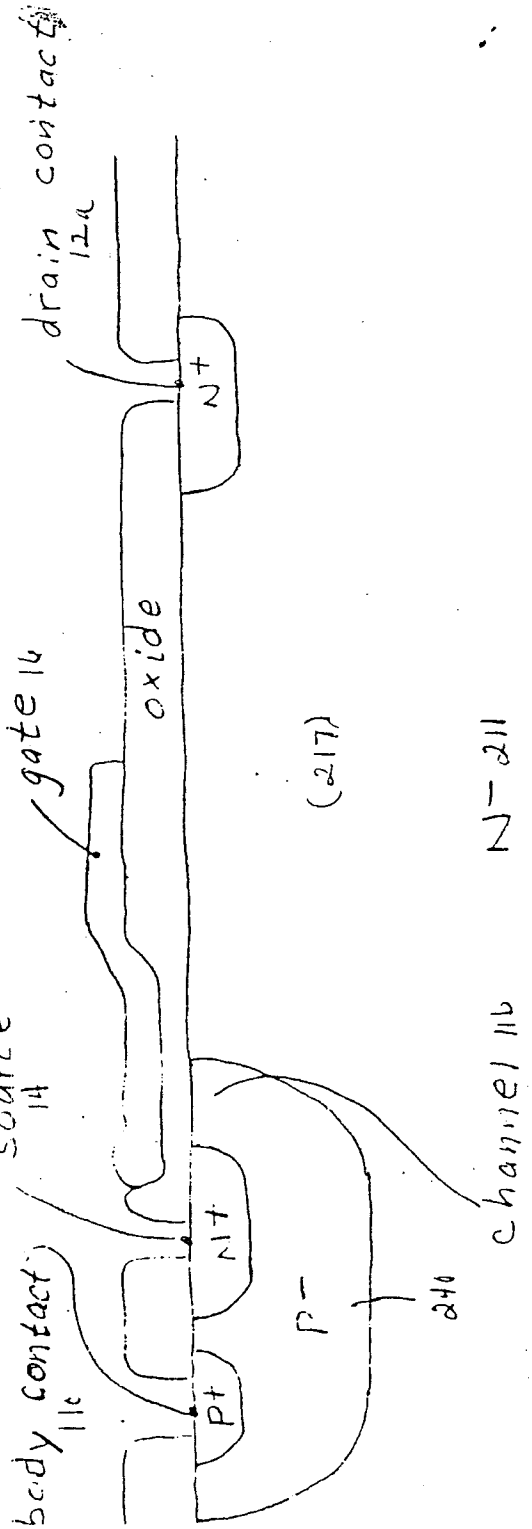
FIGURE 3



Print Of Drawings
As Originally Filed

07/705509

Lateral DMOS prior art



Print Of Drawings
As Originally Filed

FIGURE 4

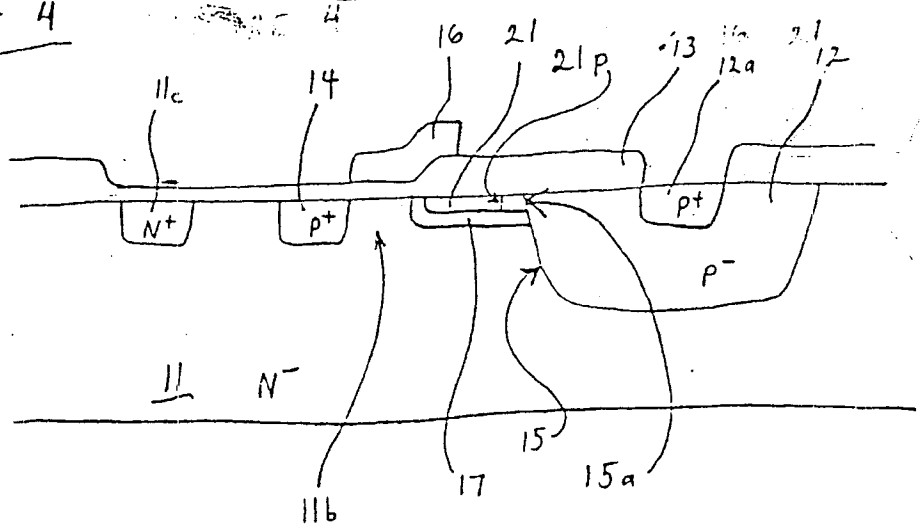
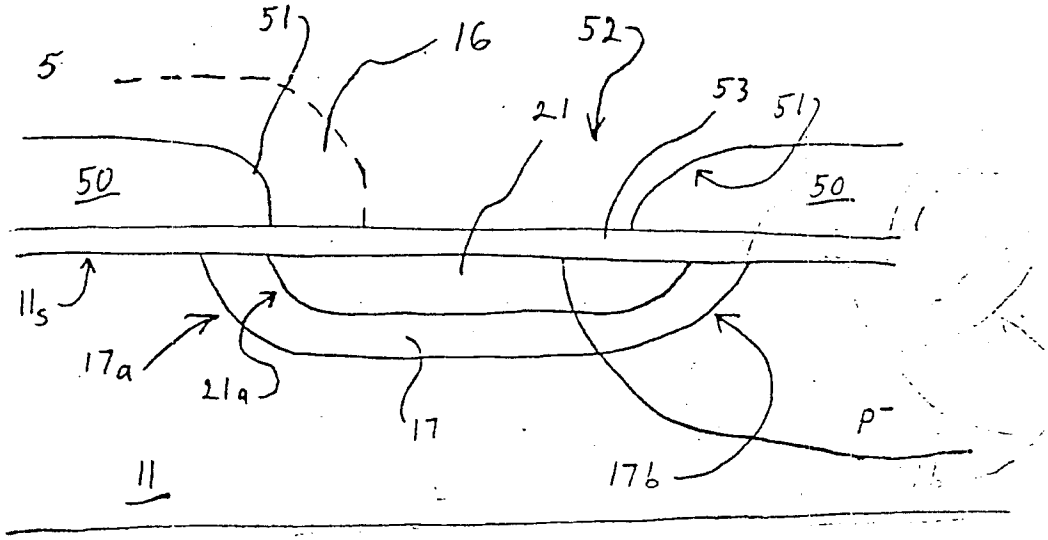


FIGURE 5



Print Of Drawings
As Originally Filed

07/705509

FIGURE 6a

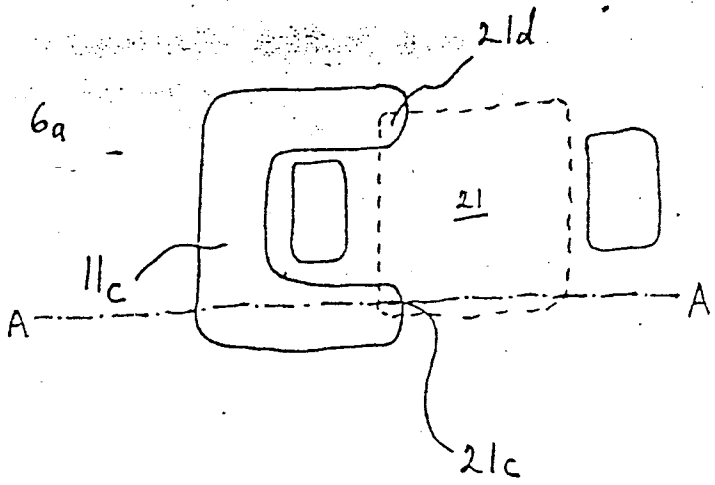
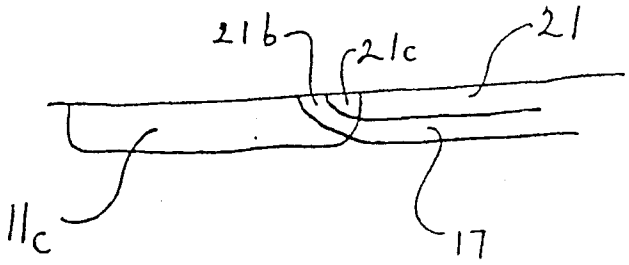


FIGURE 6b



Print Of Drawings
As Originally Filed

07/705509

IGURE 7

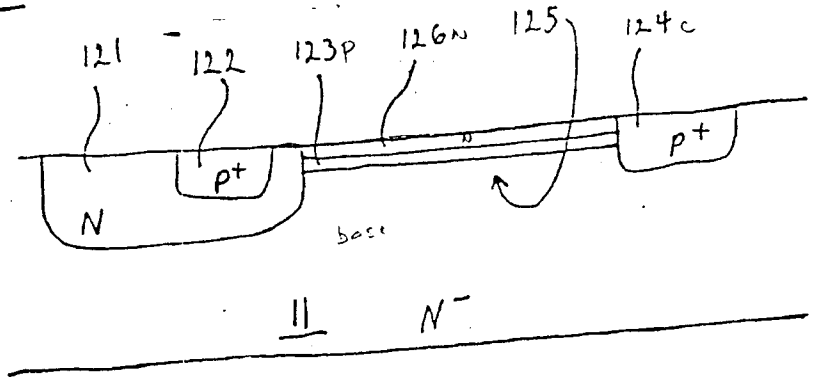
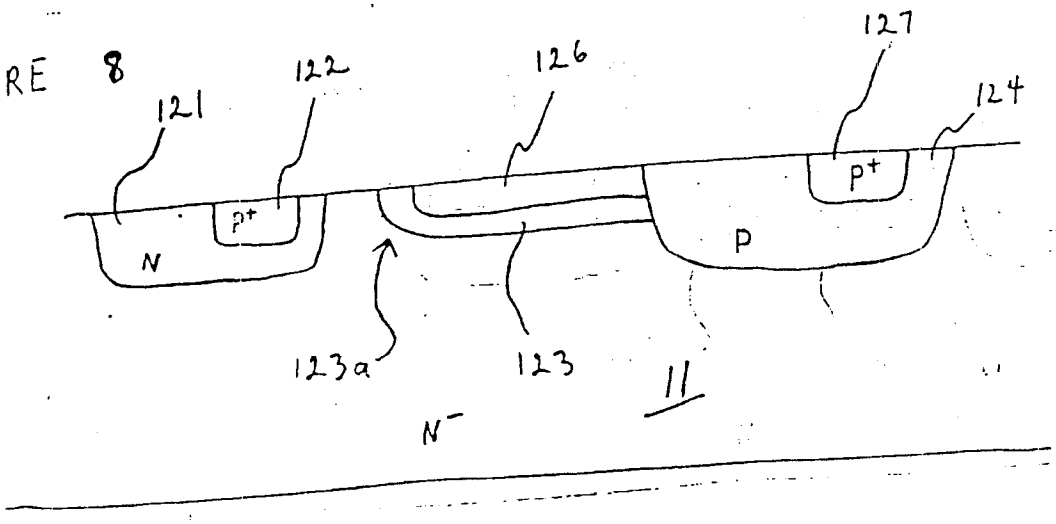


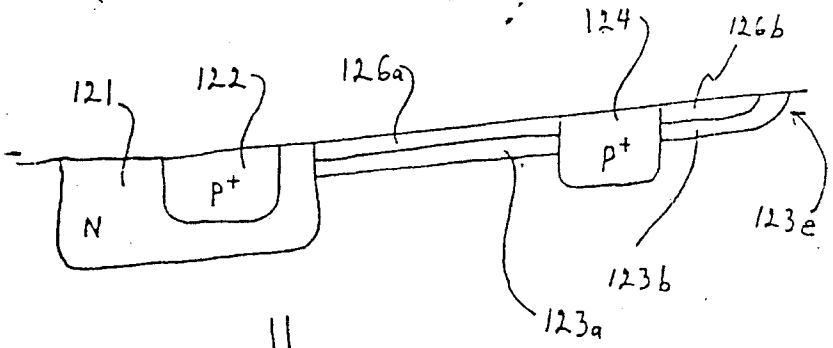
FIGURE 8



Print Of Drawings
As Originally Filed

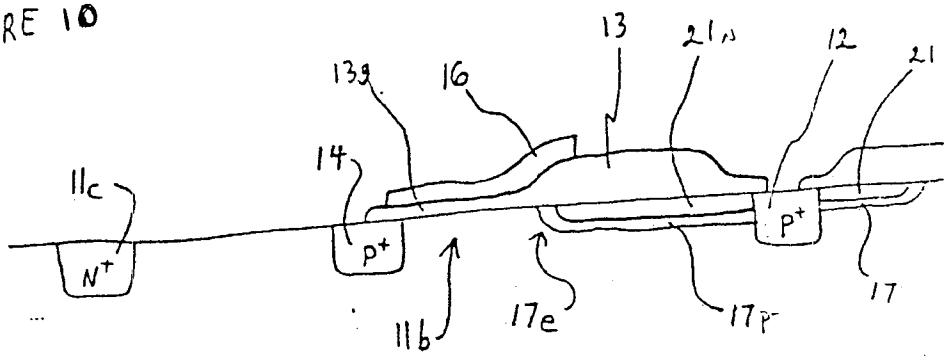
07/705509

FIGURE 9



11

FIGURE 10

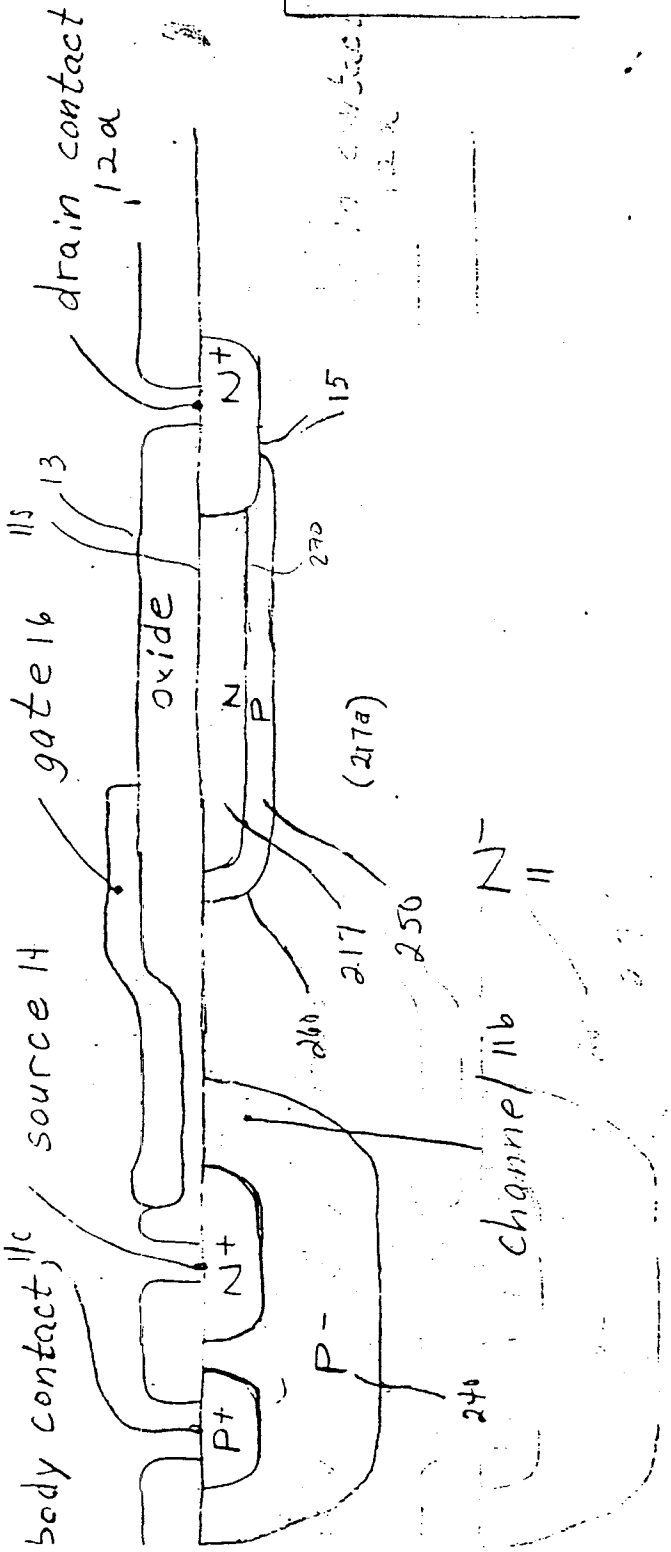


11

Print Of Drawings
As Originally Filed

IV/705509

Fig 11 high voltage LDMOS



Print Of Drawings
As Originally Filed

07/705509

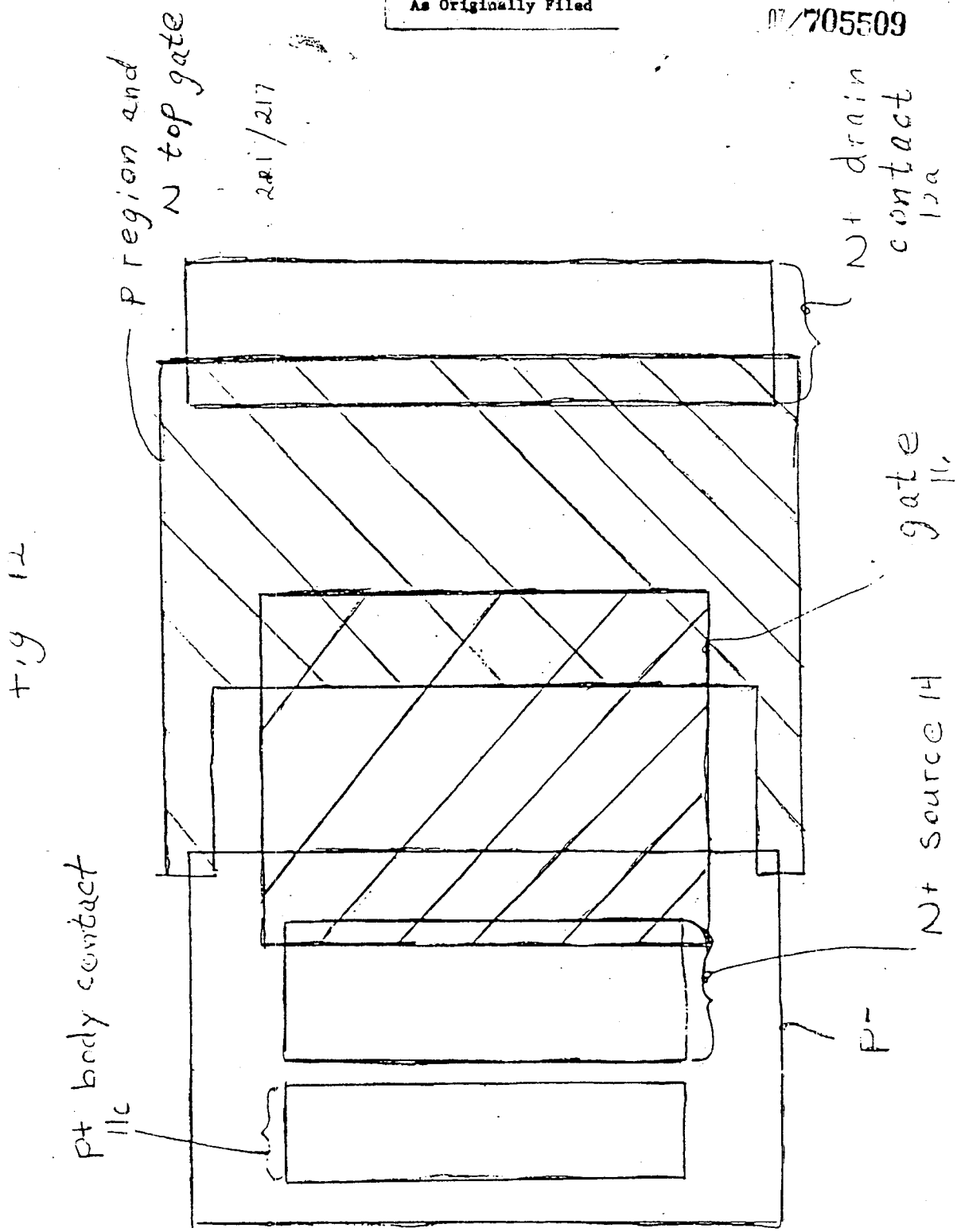


Fig 12

Print Of Drawings
As Originally Filed

07/705509

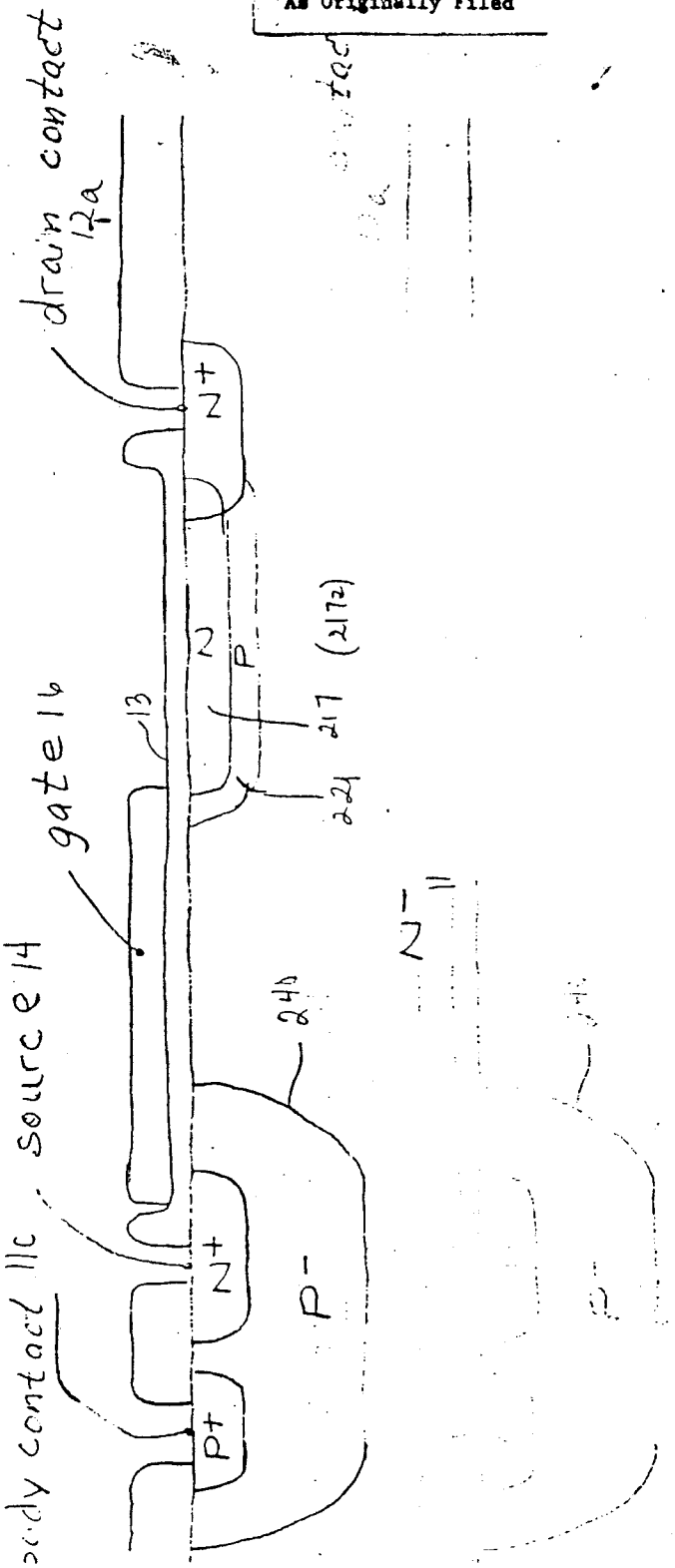


Fig 13

Print Of Drawings
As Originally Filed

705509

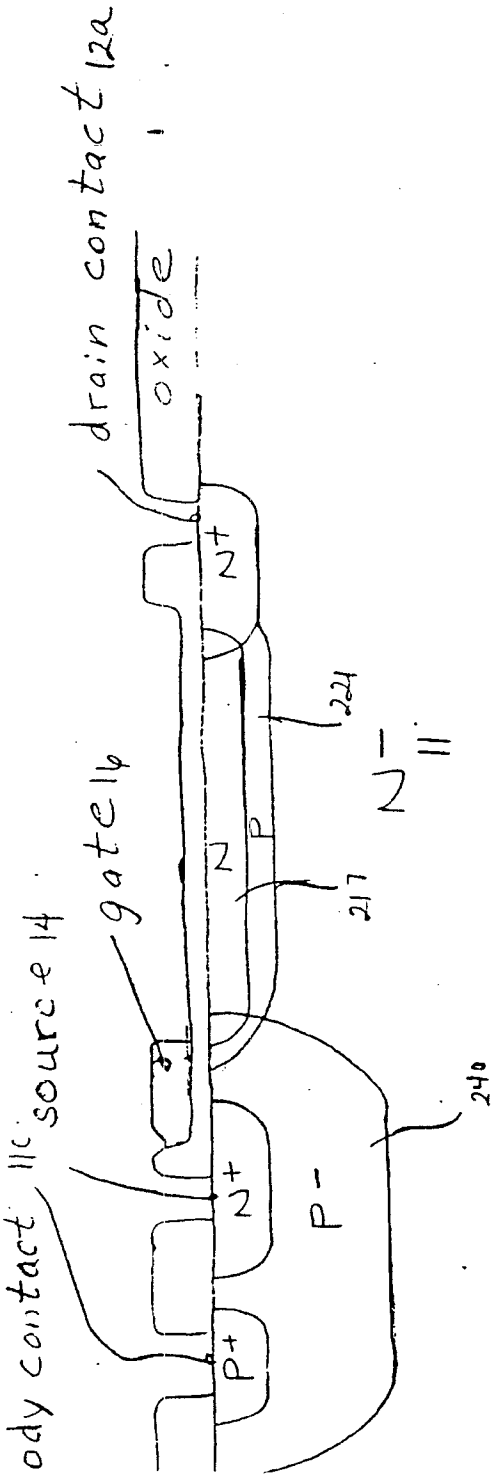


Fig 14

I hereby certify that this document is being deposited with the United States Postal Service "EXPRESS MAIL POST OFFICE TO ADDRESSEE" service under 37 CFR 1.10 and addressed to the Commissioner of Patents and Trademarks, Washington, D.C. 20231.
Date: 5/24/91 By: C. Nielsen
Express Mail No.: EB733690527US

490-101-A

117705509

118/28508CO

IN THE UNITES STATES PATENT AND TRADEMARK OFFICE

Prior Application Serial No.: 242,405
Filed: September 8, 1988 - pending;
Title: HIGH VOLTAGE LATERAL SEMICONDUCTOR DEVICE
Inventor: James D. Beasom
Group: 258
Examiner: R. Potter

Honorable Commissioner of
Patents and Trademarks
Washington, DC 20231

May 24, 1991

Sir:

This is a request for filing a _X_ Continuation _____ Divisional application under 37 CFR 1.60, of pending application, Serial No. 242,405, filed September 8, 1988, of James D. Beasom for HIGH VOLTAGE LATERAL SEMICONDUCTOR DEVICE.

_X_ 1. Enclosed is a copy of the prior application as originally filed, and an affidavit or declaration verifying it as a true copy is incorporated herein.

_X_ 2. The filing fee is calculated below:

CLAIMS AS FILED, LESS ANY CLAIMS CANCELED BY AMENDMENT

For	Number Filed	Number Extra	Rate	Basic Fee $ 630.00
Total claims:	42 - 20 =	22	x $20	$ 440.00
Independent claims:	10 - 3 =	7	x $60	$ 420.00

Total Filing Fee: $1490.00 attached hereto.

_x_ 3. To the extent necessary, Applicant petitions for an extension of time under 37 CFR 1.136. Please charge any shortage in fees or credit any overpayment thereof, including extension of time fees to Account No.05-1323 (118/28508CO). A duplicate copy of this sheet is attached.

_x_ 4. Cancel original claims 2-30 of the prior application before calculating the filing fee.

__X__ 5. Amend the specification by inserting the following before the first line thereof:

--This is a __X__ continuation _____ division of Application Serial No. 242,406, filed September 8, 1988 - pending.

_____ 6. Transfer the drawings from the prior application to the instant application and abandon said prior application as of the filing date accorded this application. A duplicate copy of this sheet is enclosed for filing in the prior application file.

_____ 6a. New formal drawings are enclosed.

__X__ 6b. Informal drawings are enclosed.

_____ 7. Priority is claimed under 35 USC 119 based upon Application No.

_____ 7a. The certified copy was filed on * in prior application, Serial No. * filed *.

__X__ 8. The prior application is assigned of record to: Harris Corporation of Melbourne, Florida. A copy of the Assignment document is attached.

__X__ 9. The power of attorney in the prior application is to:

William A. Troner, Reg. No. 32,316 et al;

and a new APPOINTMENT OF ASSOCIATE ATTORNEY was filed in the prior application to:

Charles E. Wands, Reg. no. 25,649 et al.

__X__ 9a. The power appears in the original papers in the prior application.

__X__ 9b. A copy of the power in the prior application is enclosed, along with a copy of the APPOINTMENT OF ASSOCIATE ATTORNEY.

__X__ 10. Address all future communications in connection with this application to:

EVENSON, WANDS, EDWARDS, LENAHAN & MCKEOWN
25240 Babcock Street, NE, Suite 206
Palm Bay, Florida 32905

__X__ 11. A Preliminary Amendment is enclosed. (Any claims added by the Preliminary Amendment have been properly numbered consecutively beginning with the number next following the highest numbered original claim in the prior application.)

__X__ 12. I hereby verify that the attached papers are a true copy of the prior application Serial No. 242,405, originally filed in the U.S. Patent and Trademark Office on September 8, 1988.

The undersigned declares further that all statements made herein of his own knowledge are true and that all statements made on information and belief are believed to be true; and further, that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Respectfully submitted,

Charles E. Wands 30/
Registration No. 25,649
EVENSON, WANDS, EDWARDS, LENAHAN & MCKEOWN

Date: 24 MAY 91

CEW:cn
(407)725-4760
(202)457-9090

pat\28508.60

I hereby certify that this document is being deposited with the United States Postal Service "EXPRESS MAIL POST OFFICE TO ADDRESSEE" service under 37 CFR 1.10 and addressed to the Commissioner of Patents and Trademarks, Washington, D.C. 20231.
Date: 5/24/91 By: C. Williams
Express Mail No.: FB123698 7XUS

07/705509

1/2

118/28508CO

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT: James D. Beasom

SERIAL NO.: Rule 60 Continuation Application of USSN: 242,405, Filed: September 8, 1988

FOR: HIGH VOLTAGE LATERAL SEMICONDUCTOR DEVICE

Honorable Commissioner of
Patents and Trademarks
Washington, D.C. 20231

May 24, 1991

PRELIMINARY AMENDMENT

Sir:

Preliminary to the examination of the above-identified application, the following Amendments and Remarks are respectfully submitted.

IN THE SPECIFICATION:

Page 2, eighth line from the bottom, change "drain body" to --drain-to-body--;

Page 3, line 4, change "channel body" to --channel-to-body--;

Page 3, fourth line from the bottom, change "12" to --contact 12A--;

Page 4, first full paragraph, fifth line, change "body drain" to --body-to-drain--;

Page 9, tenth line from the bottom, change "drain body" to --drain-to-body--;

Page 9, fourth line from the bottom, change "gate to drift" to --gate-to-drift--; after "junction", insert --17A--; after "gate" (last occurrence), insert --21--;

Page 10, top paragraph, line 2, after "channel", insert --17--;

Page 10, line 5, change "body to drain" to --body-to-drain--;

Page 10, line 6, change "gate to channel" to --gate-to-channel--;

Page 10, line 7, change "additon" to --addition--;

Page 10, line 13, after "region", insert --17--;

Page 10, bottom paragraph, line 3, change "body to drain" to --body-to-drain--;

Page 10, bottom paragraph, line 4, change "gate to drain" to --gate-to-drain--;

Page 10, bottom paragraph, line 5, after "11", insert --(as shown in Figures 6A, 6B to be described below)--; change "gate to drain" to --gate-to-drain--;

Page 11, line 1, change "body to drain" to --body-to-drain--;

Page 11, line 2, change "gate to drain" to --gate-to-drain--;

Page 11, second paragraph, line 3, after "region", insert --17--;

Page 11, second paragraph, line 6, after "and", insert --N--;

Page 11, second paragraph, line 8, change "effected" to --affected--;

Page 12, line 1, after "and", insert --,--;

Page 12, line 2, after ")", insert --,--;

Page 12, line 9, change "ion implanted" to --ion-implanted--;

Page 12, second paragraph, line 3, after "channel" (first occurrence), insert --17--;

Page 13, line 1, after "region", insert --17--; after "gate", insert --21--";

Page 13, line 2, after "oxide", insert --53--;

Page 13, line 13, after "gate" (last occurrence), insert --21--;

Page 14, line 7, after "17", insert --,--;

Page 14, second paragraph, line 8, change "so" to --as--;

Page 14, second paragraph, line 11, after "11", insert --, via contact region 11C--;

Page 15, first full paragraph, line 4, before "top", insert --N type--;

Page 15, line 8, change "gate to drift" to --gate-to-drift--;

Page 15, line 9, after "region" (last occurrence), insert --123--;

Page 15, line 10, after "negative", insert --,--;

Page 16, bottom paragraph, first line, change "base to" to --base-to--";

Page 16, bottom paragraph, line 4, after "gate", insert --126A--; after "region" (last occurrence), insert --123A--;

Page 16, bottom paragraph, line 6, after "region", insert --123A--;

Page 16, bottom paragraph, line 7, change "ro" to --for--;

Page 17, line 3, after "shield", insert --121--;

Page 17, first full paragraph, line 5, after "region", insert

--17--;

Page 18, first full paragraph, line 3, after "contact", insert

--11C--;

Page 18, last paragraph, line 1, change "in" to --by way of--; after "second", insert --(surface)--;

Page 18, last paragraph, line 2, change "217_a" to --217--; before "prior", insert --(deeper)--; after "region" (last occurrence), insert --217A--;

Page 18, last paragraph, line 3, change "as shown" to --, refer to above--;

Page 18, last paragraph, line 4, after "region", insert --11--; before "layer", insert --top gate--;

Page 19, line 2, change "region" to --body 11--;

Page 19, line 3, after "layers", insert --217, 250 respectively--;

Page 19, first full paragraph, line 3, change "region" to --body 11--;

Page 19, first full paragraph, line 4, change "region" to --first drift region 217--;

Page 19, first full paragraph, line 6, after "contact", insert

--12A--; change "region" to --body 11--;

Page 19, first full paragraph, line 7, change "drain body" to --drain-to-body--;

Page 19, first full paragraph, line 8, before "region", insert --first drift--;

Page 20, line 3, change "layer" to --first drift region--;

Page 20, line 4, change "layer" (first occurrence) to --first drift region--; change "layer" (last occurrence" to --region--;

Page 20, line 5, change "layer" to --region 250--;

Page 20, first full paragraph, line 2, change "drain body" to --drain-to-body--;

Page 20, first full paragraph, line 3, after "junction", insert --15--; change "P and N-" to --P N- --;

Page 20, first full paragraph, line 4, change "P to N" to --P N--; change "N and " to --N first drift region 217 and--;

Page 20, first full paragraph, line 5, change "regions" to --body 11--; after "layer", insert --250--;

Page 20, first full paragraph, line 6, change "layer" to --first drift region--;

Page 21, line 4, change "layer" to --first drift region--;

Page 21, first full paragraph, line 2, change "layers" to --regions--; change "250" to --221--;

Page 21, last paragraph, line 2, change "250" to --221--;